MOTOROLA

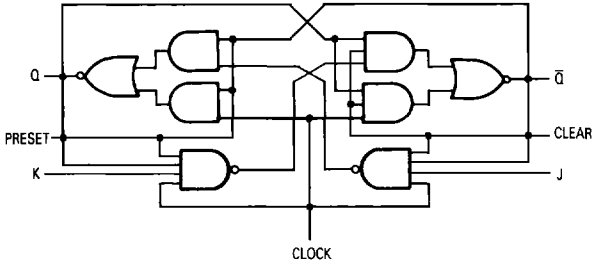
Military 54LS76A

Dual J-K Flip-Flop With Clear and Preset

ELECTRICALLY TESTED PER:
MIL-M-38510/30110

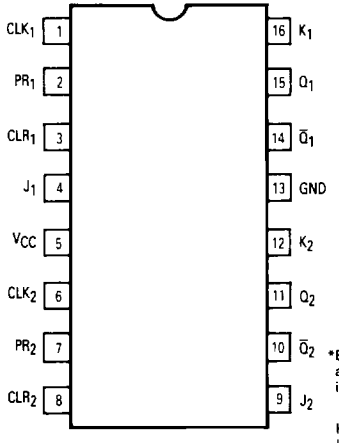
The 54LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH to LOW clock pulse.

LOGIC DIAGRAM
(one half show)

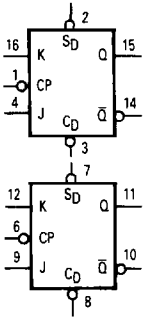


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CONNECTION DIAGRAM



LOGIC SYMBOL



*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AVAILABLE AS:

1) JAN: JM38510/30110BXA
2) SMD: 7601301
3) 883C: 54LS76A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: SEE 54LS112A
***Call Factory for latest update**

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION A)
CLK_1	1	1	V_{CC}
PR_1	2	2	GND
CLR_1	3	3	GND
J_1	4	4	V_{CC}
V_{CC}	5	5	V_{CC}
CLK_2	6	6	V_{CC}
PR_2	7	7	GND
CLR_2	8	8	GND
J_2	9	9	V_{CC}
$\overline{Q}_2$	10	10	V_{CC}
Q_2	11	11	V_{CC}
K_2	12	12	V_{CC}
GND	13	13	GND
$\overline{Q}_1$	14	14	V_{CC}
Q_1	15	15	V_{CC}
K_1	16	16	V_{CC}

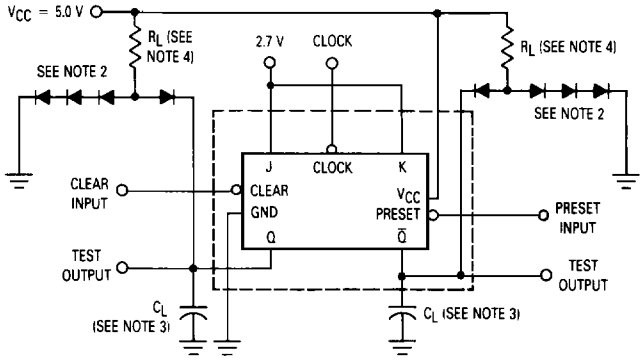
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

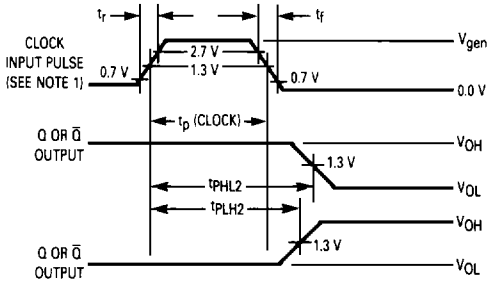
6

AC TEST CIRCUIT



Synchronous Switching Test Circuit

WAVEFORMS

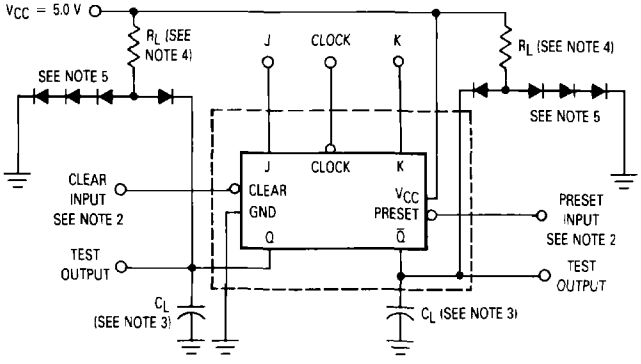


NOTES:
1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output): V_{gen} = 3.0 V, $t_r \leq$ 15 ns, $t_f \leq$ 6.0 ns, t_p (clock) = 25 ns and PRR ≤ 1.0 MHz. When testing f_{MAX} the clock input characteristics are: V_{gen} = 3.0 V, $t_r = t_f \leq$ 6.0 ns, t_p (clock) ≤ 20 ns and PRR = (see table 1).
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.

6

AC TEST CIRCUIT

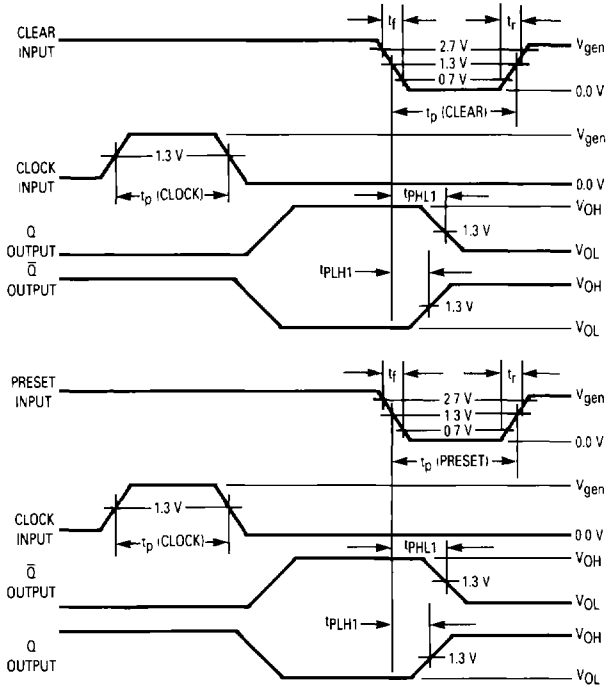
Clear Switching Test Circuit and Waveforms



NOTES:

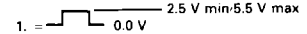
1. Clear or preset inputs dominate regardless of the state of clock J-K inputs.
2. Clear or preset input pulse characteristics: V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, t_p (clear) = t_p (preset) = 30 ns, $Z_{out} \approx 50\ \Omega$.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.
5. All diodes are 1N3064, or equivalent.
6. When testing clear to output switching, preset shall have a logical "1" voltage applied. When testing preset to output switching, clear input shall have a logical "1" voltage applied (see table 1).
7. Clock input pulse characteristics: t_p (clock) ≥ 25 ns, V_{gen} = 3.0 V, PRR ≤ 1.0 MHz.

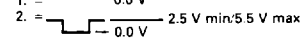
WAVEFORMS



Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH1}	Logical "1" Input Current (J & K inputs)		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, PR & K = 4.5 V, CLK & CLR = 0 V.
I_{IHH1}	Logical "1" Input Current (J & K inputs)		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, CLR & J = 4.5 V, CLK & PR = 0 V.
I_{IH2}	Logical "1" Input Current (CLR & PR)		60		60		60	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, K = 4.5 V, CLK & CLR = GND, PR = (See Note 2).
I_{IHH2}	Logical "1" Input Current (CLR & PR)		300		300		300	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, J = 4.5 V, CLK & K = GND, CLR = (See Note 2).
I_{IH3}	Logical "1" Input Current (CLK inputs)		80		80		80	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = GND.
I_{IHH3}	Logical "1" Input Current (CLK inputs)		400		400		400	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = GND.
I_{IL1}	Logical "0" Input Current (J & K inputs)	−0.12	−0.36	−0.12	−0.36	−0.12	−0.36	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CLK = CLR & J = 4.5 V, PR = (See Note 2).
I_{IL2}	Logical "0" Input Current (CLK & inputs)	−0.24	−0.72	−0.24	−0.72	−0.24	−0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, PR = J & K = 4.5 V, CLR = (See Note 2).
I_{IL3}	Logical "0" Input Current (PR inputs)	−0.12	−0.72	−0.12	−0.72	−0.12	−0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs = GND, V_{OUT} = 0 V.
I_{CC}	Power Supply Current		8.0		8.0		8.0	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, or V_{IN} = 5.5 V, other inputs = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. 

2. 

6

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Switching Parameters	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output CLR_n or PR_n to Q_n	5.0	28 20	5.0	40 35	5.0	40 35	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output CLR_n or PR_n to Q_n	5.0	21 20	5.0	32 27	5.0	32 27	ns ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output CLK_n to Q_n	5.0	30	5.0	42	5.0	42	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output CLK_n to Q_n	5.0	22	5.0	32	5.0	32	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	30						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:
1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.

6